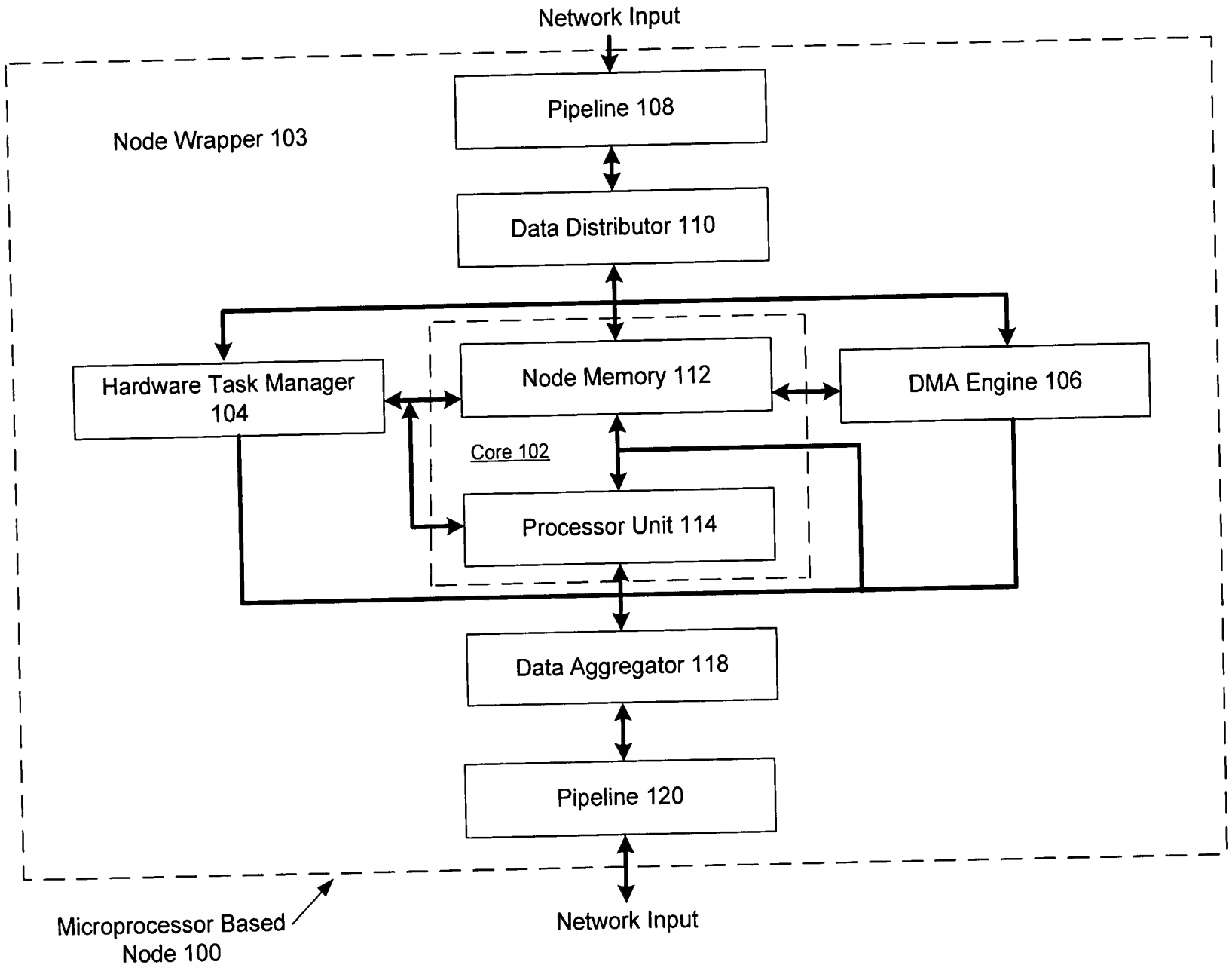
Network Input
Pipeline 108
Node Wrapper 103
Data Distributor 110
Hardware Task Manager 104
Node Memory 112
DMA Engine 106
Core 102
Processor Unit 114
Data Aggregator 118
Pipeline 120
Network Input
Microprocessor Based Node 100

Figure 1

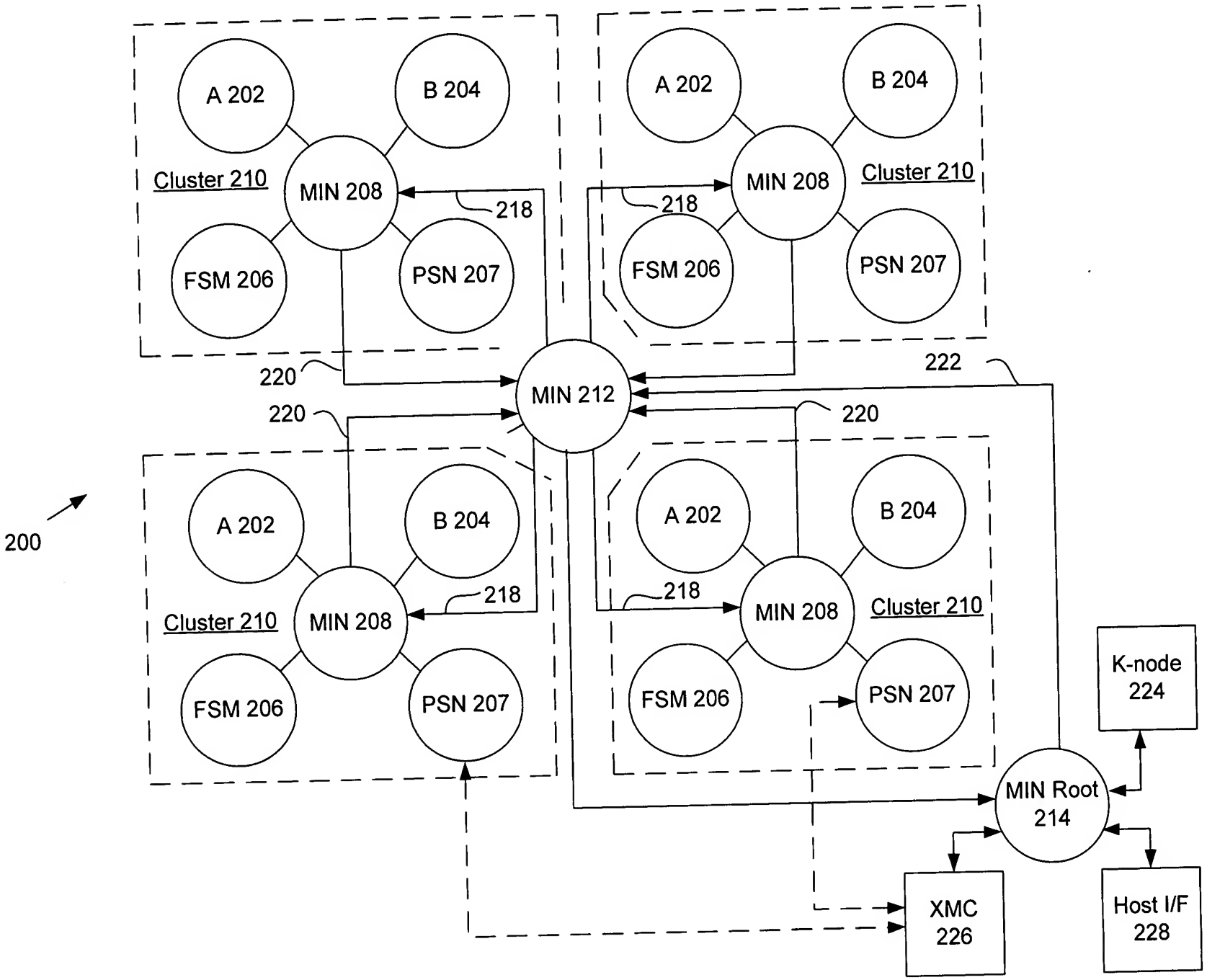
200
A 202
B 204
Cluster 210
MIN 208
218
FSM 206
PSN 207
220
MIN 212
222
K-node 224
MIN Root 214
XMC 226
Host I/F 228

FIGURE 2

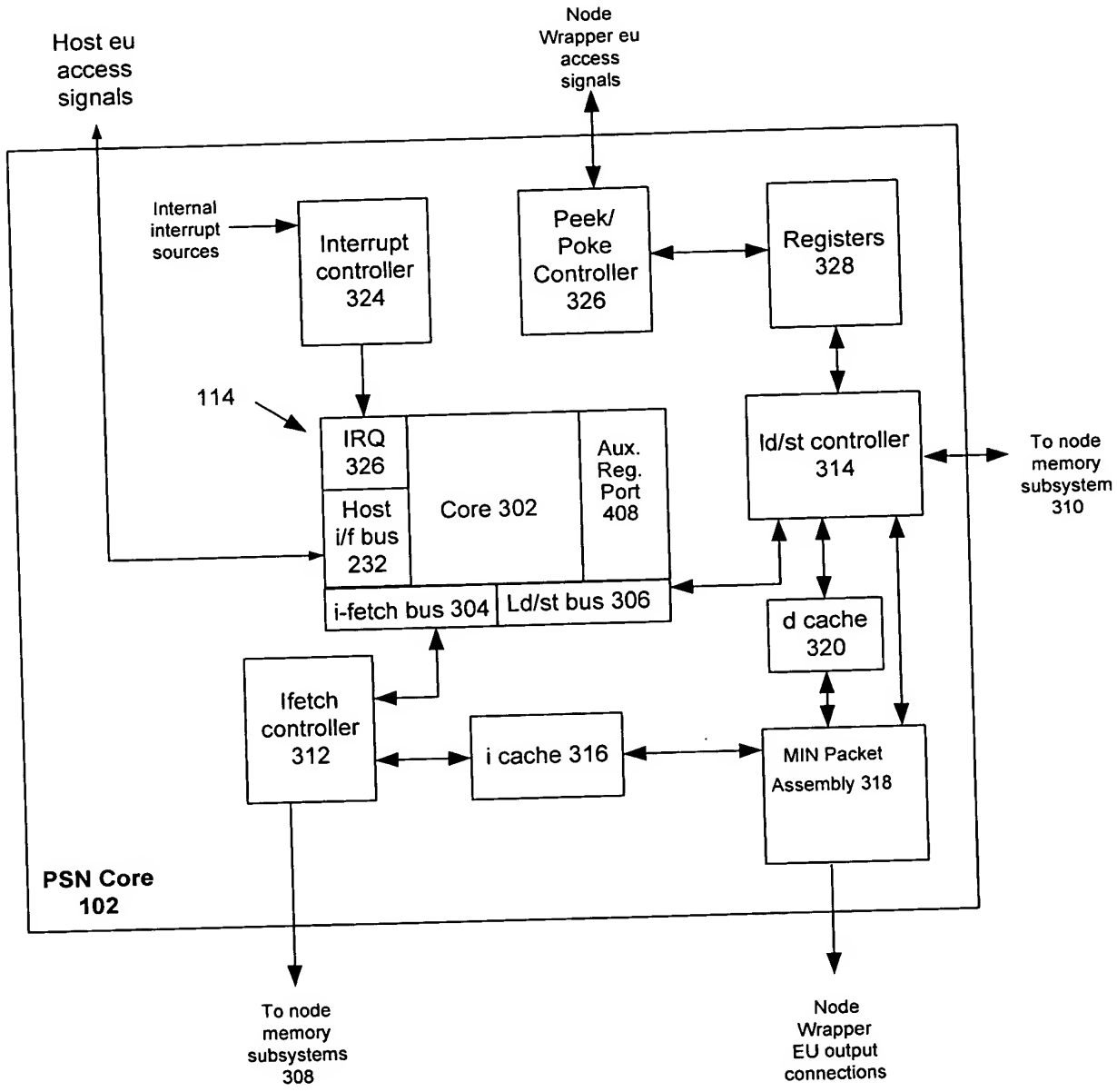
Host eu access signals
Node Wrapper eu access signals
Internal interrupt sources
Interrupt controller 324
Peek/ Poke Controller 326
Registers 328
114
IRQ 326
Host i/f bus 232
Core 302
Aux. Reg. Port 408
i-fetch bus 304
Ld/st bus 306
ld/st controller 314
To node memory subsystem 310
d cache 320
Ifetch controller 312
i cache 316
MIN Packet Assembly 318
PSN Core 102
To node memory subsystems 308
Node Wrapper EU output connections

Figure 3

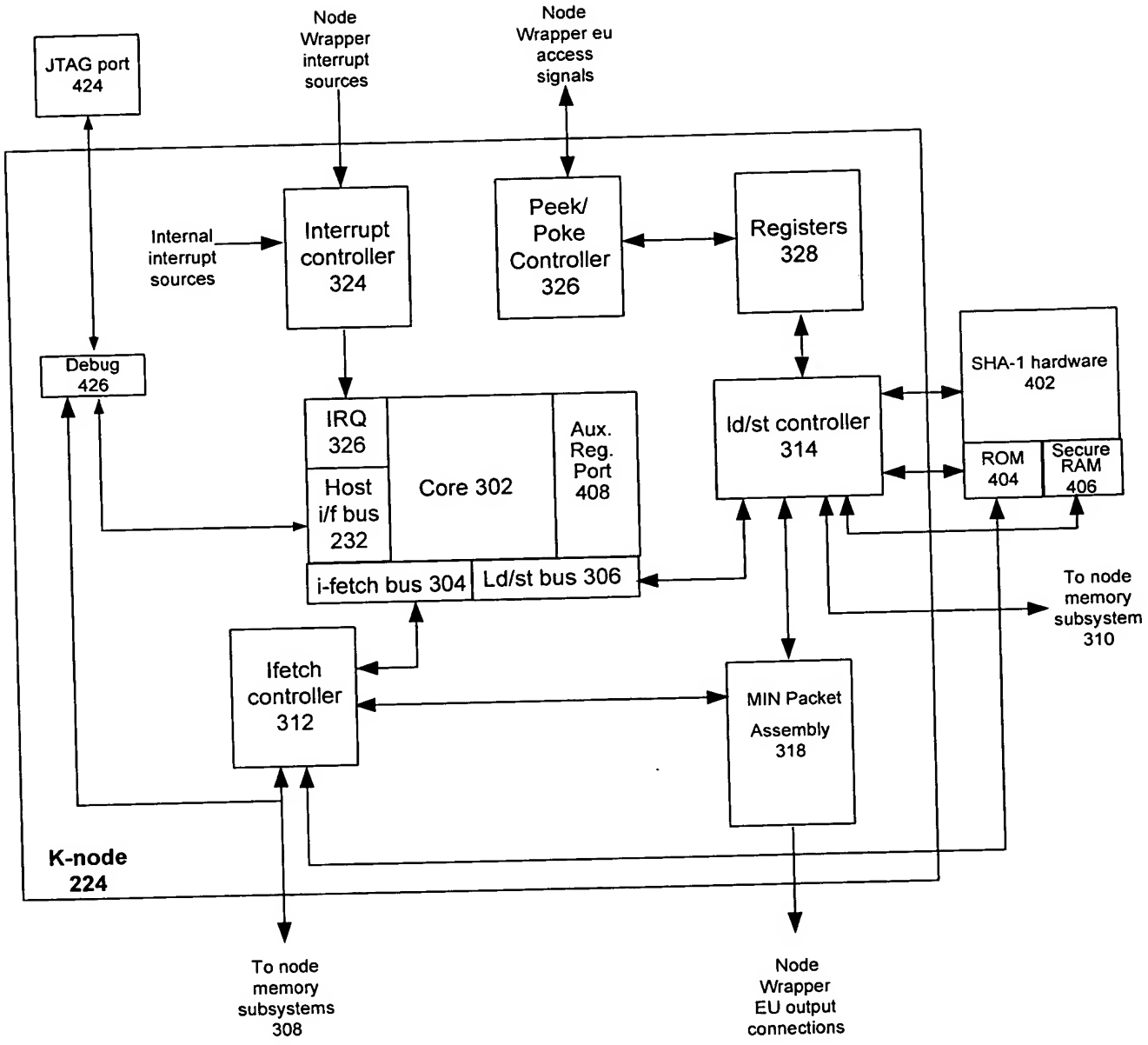
JTAG port 424
Node Wrapper interrupt sources
Node Wrapper eu access signals
Internal interrupt sources
Interrupt controller 324
Peek/ Poke Controller 326
Registers 328
Debug 426
IRQ 326
Host i/f bus 232
Core 302
Aux. Reg. Port 408
i-fetch bus 304
Ld/st bus 306
ld/st controller 314
SHA-1 hardware 402
ROM 404
Secure RAM 406
To node memory subsystem 310
Ifetch controller 312
MIN Packet Assembly 318
K-node 224
To node memory subsystems 308
Node Wrapper EU output connections

Figure 4

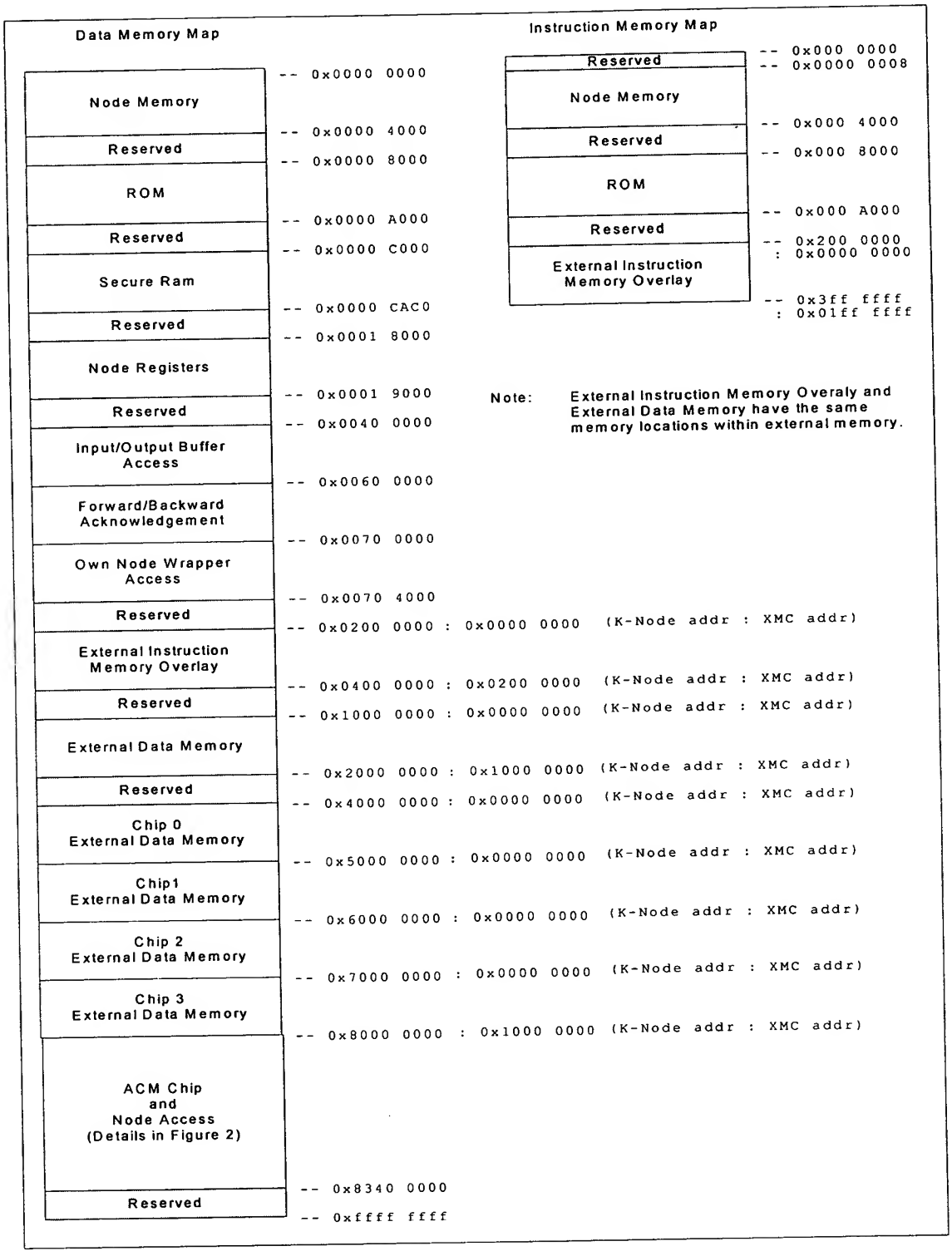
Data Memory Map
Node Memory
-- 0x0000 0000
Reserved
-- 0x0000 4000
ROM
-- 0x0000 8000
Reserved
-- 0x0000 A000
Secure Ram
-- 0x0000 C000
Reserved
-- 0x0000 CAC0
Node Registers
-- 0x0001 8000
Reserved
-- 0x0001 9000
Input/Output Buffer Access
-- 0x0040 0000
Forward/Backward Acknowledgement
-- 0x0060 0000
Own Node Wrapper Access
-- 0x0070 0000
Reserved
-- 0x0070 4000
External Instruction Memory Overlay
-- 0x0200 0000 : 0x0000 0000 (K-Node addr : XMC addr)
Reserved
-- 0x0400 0000 : 0x0200 0000 (K-Node addr : XMC addr)
External Data Memory
-- 0x1000 0000 : 0x0000 0000 (K-Node addr : XMC addr)
Reserved
-- 0x2000 0000 : 0x1000 0000 (K-Node addr : XMC addr)
Chip 0 External Data Memory
-- 0x4000 0000 : 0x0000 0000 (K-Node addr : XMC addr)
Chip1 External Data Memory
-- 0x5000 0000 : 0x0000 0000 (K-Node addr : XMC addr)
Chip 2 External Data Memory
-- 0x6000 0000 : 0x0000 0000 (K-Node addr : XMC addr)
Chip 3 External Data Memory
-- 0x7000 0000 : 0x0000 0000 (K-Node addr : XMC addr)
ACM Chip and Node Access (Details in Figure 2)
-- 0x8000 0000 : 0x1000 0000 (K-Node addr : XMC addr)
Reserved
-- 0x8340 0000
-- 0xffff ffff
Instruction Memory Map
Reserved
-- 0x000 0000
-- 0x0000 0008
Node Memory
-- 0x000 4000
Reserved
-- 0x000 8000
ROM
-- 0x000 A000
Reserved
-- 0x200 0000
: 0x0000 0000
External Instruction Memory Overlay
-- 0x3ff ffff
: 0x01ff ffff
Note: External Instruction Memory Overaly and External Data Memory have the same memory locations within external memory.

Figure 5A

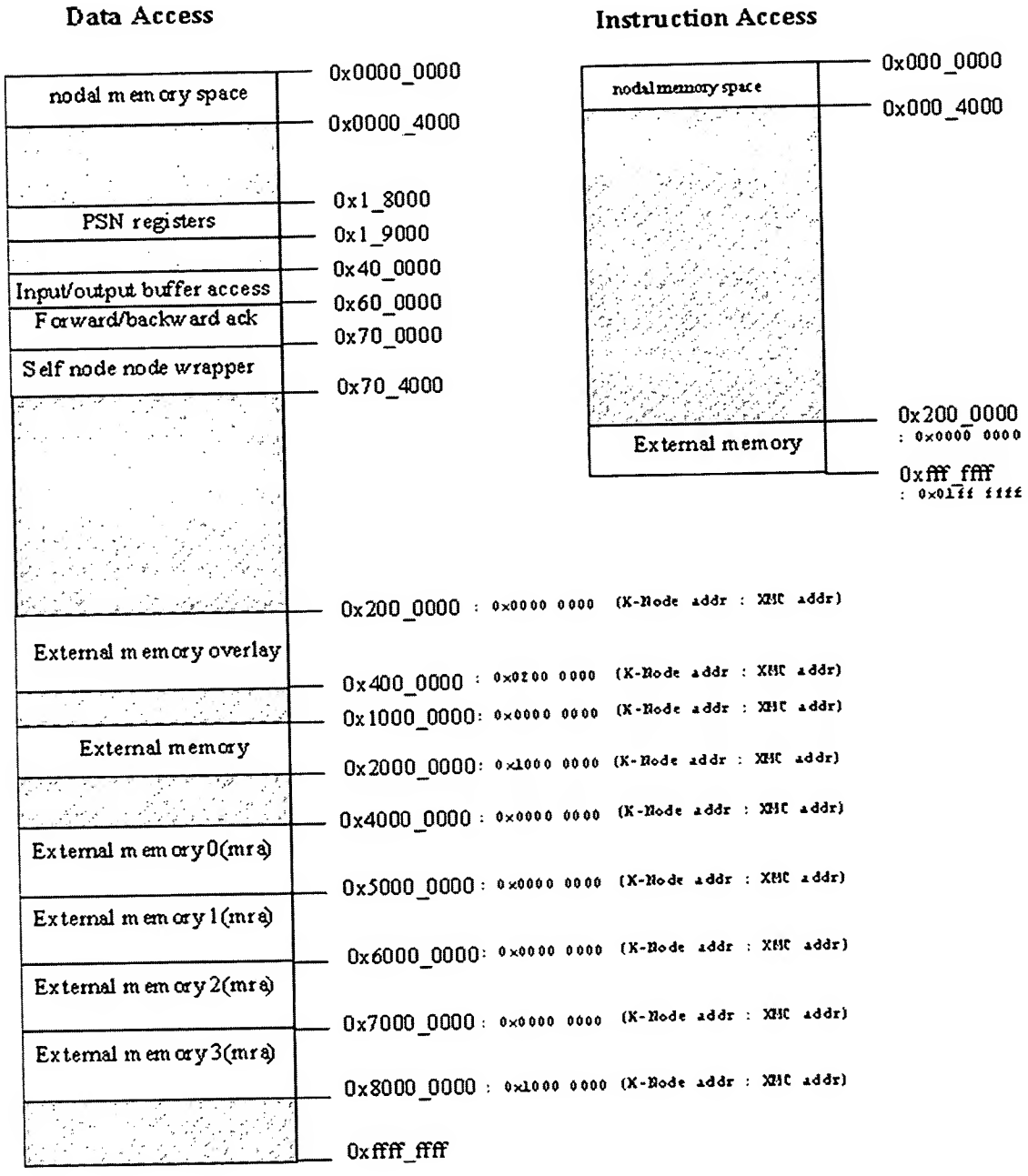
Data Access
nodal memory space
0x0000_0000
0x0000_4000
PSN registers
0x1_8000
0x1_9000
Input/output buffer access
0x40_0000
0x60_0000
Forward/backward ack
0x70_0000
Self node node wrapper
0x70_4000
0x200_0000 : 0x0000 0000 (X-Node addr : XMC addr)
External memory overlay
0x400_0000 : 0x0200 0000 (X-Node addr : XMC addr)
0x1000_0000: 0x0000 0000 (X-Node addr : XMC addr)
External memory
0x2000_0000: 0x1000 0000 (X-Node addr : XMC addr)
0x4000_0000 : 0x0000 0000 (X-Node addr : XMC addr)
External memory0(mra)
0x5000_0000 : 0x0000 0000 (X-Node addr : XMC addr)
External memory1(mra)
0x6000_0000: 0x0000 0000 (X-Node addr : XMC addr)
External memory2(mra)
0x7000_0000 : 0x0000 0000 (X-Node addr : XMC addr)
External memory3(mra)
0x8000_0000 : 0x1000 0000 (X-Node addr : XMC addr)
0xffff_ffff
Instruction Access
nodal memory space
0x000_0000
0x000_4000
External memory
0x200_0000
: 0x0000 0000
0xfff_ffff
: 0x01ff ffff

Figure 5B

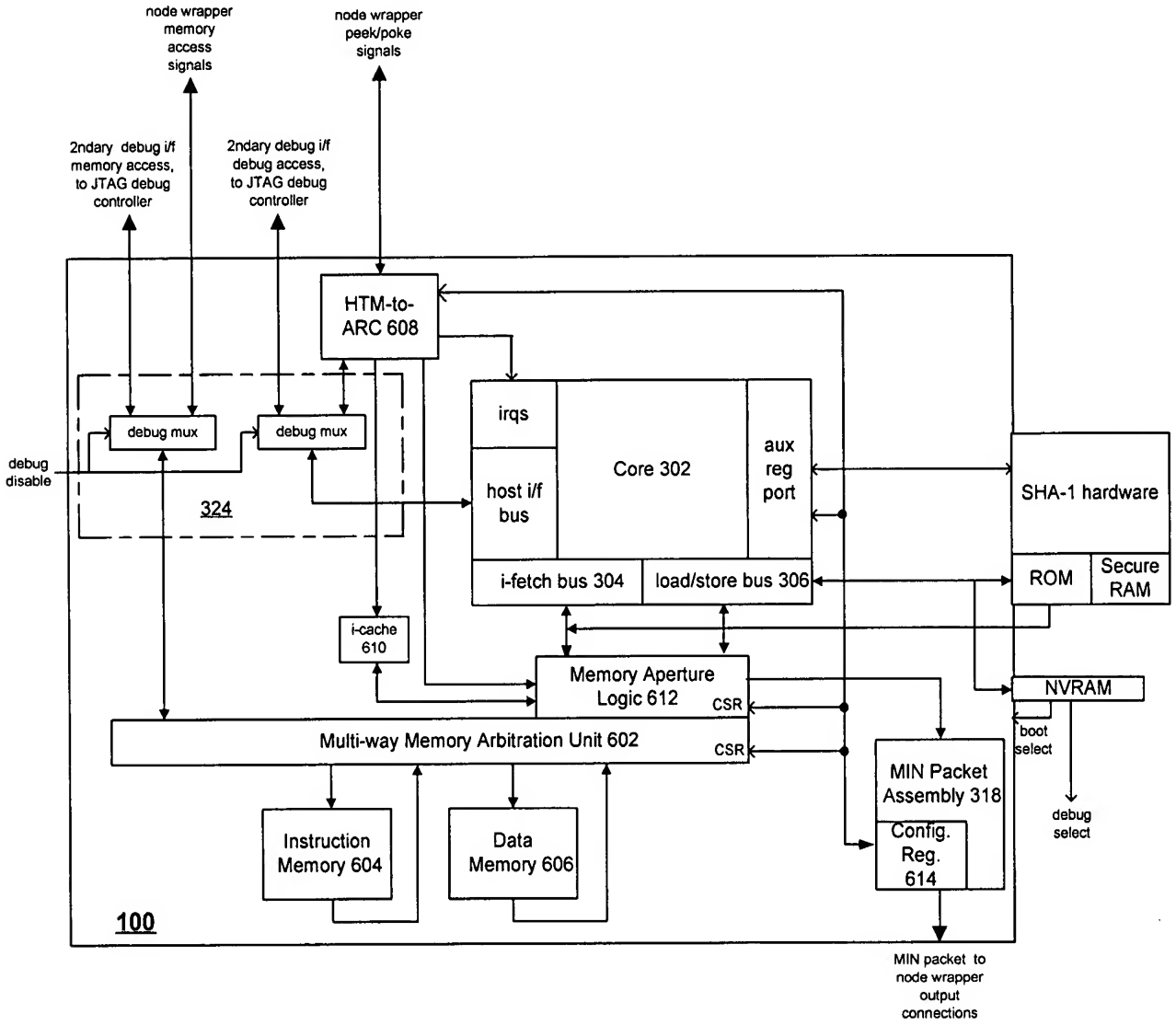
node wrapper memory access signals
node wrapper peek/poke signals
2ndary debug i/f memory access, to JTAG debug controller
2ndary debug i/f debug access, to JTAG debug controller
HTM-to-ARC 608
debug mux
debug mux
debug disable
324
irqs
host i/f bus
Core 302
aux reg port
SHA-1 hardware
ROM
Secure RAM
i-fetch bus 304
load/store bus 306
i-cache 610
Memory Aperture Logic 612
CSR
NVRAM
boot select
Multi-way Memory Arbitration Unit 602
CSR
MIN Packet Assembly 318
debug select
Instruction Memory 604
Data Memory 606
Config. Reg. 614
100
MIN packet to node wrapper output connections

Figure 6

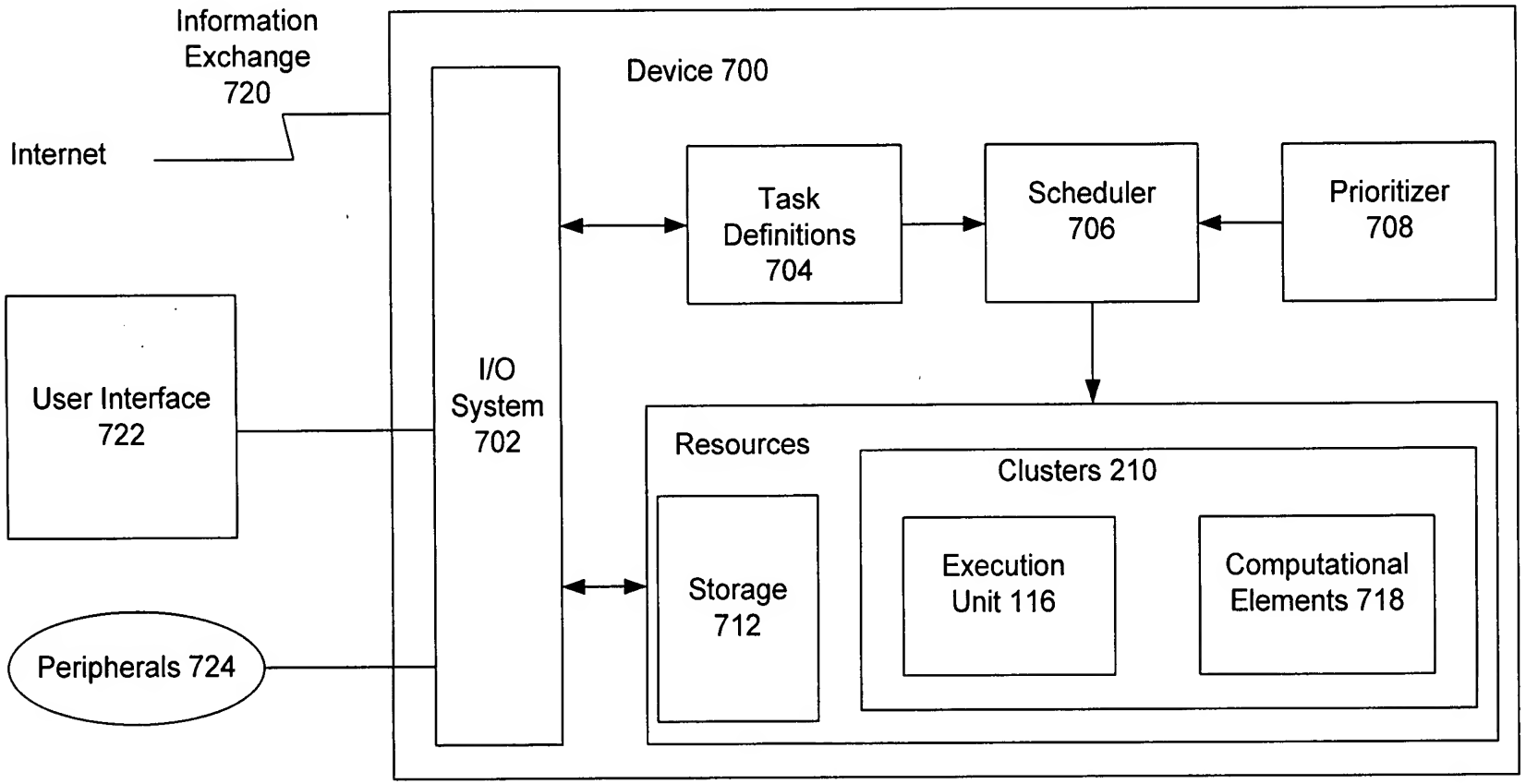
Information Exchange 720
Internet
Device 700
I/O System 702
Task Definitions 704
Scheduler 706
Prioritizer 708
User Interface 722
Resources
Clusters 210
Storage 712
Execution Unit 116
Computational Elements 718
Peripherals 724

Figure 7